CLAIMS

WHAT IS CLAIMED:

1.   A method for executing a read request over a PCI bus by transferring data from a main memory of a first device to a second device, comprising the steps of:

obtaining an access request from a queue;

transferring, by a first DMA transfer, data from said main memory to a second memory on said first device; and

transferring, by a second DMA transfer, said data from said second memory to said second device.

2.   The method of claim 1, wherein said main memory has time-variant access behavior.

3.   The method of claim 1, wherein said second memory has time-invariant access behavior.

4.   The method of claim 1, wherein said second DMA transfer is initiated and said access request is selected by a finite state machine, which is associated with said queue.

5.   The method of claim 1, wherein said second DMA transfer is initiated after said data transfer to said second memory is terminated.

6. The method of claim 1, wherein said read request is a master read request hidden as a master write access of said first device.

7. The method of claim 6, wherein said master read request is directed to a target command queue of a finite state machine.

8. The method of claim 1, wherein said second device and said main memory are decoupled.

9. The method of claim 1, wherein data polling is avoided by transforming master read cycles of said second device to master write cycles of said first device.

10. A method for executing a write request over a PCI bus by transferring requested data from a second device to a main memory of a first device, comprising the steps of:

writing an access request to a queue;

transferring, by a first DMA transfer, data from said second device to a second memory on said first device; and

transferring, by a second DMA transfer, said data from said second memory to said main memory of said first device.

11. The method of claim 10, wherein said main memory has time-variant access behavior.

12. The method of claim 11, wherein said time-variant access behavior of said main memory is taken into consideration for said second DMA transfer.

13. The method of claim 10, wherein said second memory has time-invariant access behavior.

14. The method of claim 10, wherein said first DMA transfer is initiated by said second device.

15. The method of claim 10, wherein said second DMA transfer is initiated and said access request is selected by a finite state machine, which is associated with said queue.

16. The method of claim 10, wherein said second DMA transfer is initiated after said data transfer to said second memory is terminated.

17. The method of claim 10, wherein said second device and said main memory are decoupled.

18. An apparatus for executing a read request over a PCI bus, comprising:

a queue for storing a read access request;

a main memory for storing data to be transferred;

a buffer memory for buffer storage of said data, whereby data transfer to said buffer memory is accomplished by a first DMA transfer;

a device located on the PCI bus for receiving said data, whereby data transfer from

said buffer memory to said device is accomplished by a second DMA transfer;

and

a finite state machine associated with said queue for selecting an access request.

19. The apparatus of claim 18, wherein said main memory has time-variant access behavior.

20. The apparatus of claim 18, wherein said buffer memory has time-invariant access behavior.

21. The apparatus of claim 18, wherein said main memory and said buffer memory are located on a PCI card.

22. The apparatus of claim 18, wherein said finite state machine is adapted to initiate said second DMA transfer.

23. The apparatus of claim 18, wherein said second DMA transfer is initiated after said data transfer to said buffer memory is terminated.

24. The apparatus of claim 18, wherein said device and said main memory are decoupled.

25. The apparatus of claim 21, wherein data polling is avoided by transforming master read cycles of said device to master write cycles of said PCI card.

26.   An apparatus for executing a write request over a PCI bus, comprising:

a queue for storing a write access request;

a device located on a PCI bus for storing data to be transferred;

a main memory for receiving said data;

a buffer memory for buffer storage of said data, whereby data transfer to said buffer

memory is accomplished by a first DMA transfer and data transfer from said

buffer memory to said main memory is accomplished by a second DMA

transfer; and

a finite state machine associated with said queue for selecting an access request.

27.   The apparatus of claim 26, wherein said main memory has time-variant access

behavior.

28.   The apparatus of claim 27, wherein said time-variant access behavior of said

main memory is taken into consideration for said second DMA transfer.

29.   The apparatus of claim 26, wherein said buffer memory has time-invariant

access behavior.

30.   The apparatus of claim 26, wherein said main memory and said buffer

memory are located on a PCI card.

31.   The apparatus of claim 26, wherein said first DMA transfer is initiated by said

device.

32.   The apparatus of claim 26, wherein said finite state machine is adapted to initiate said second DMA transfer.

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33.   The apparatus of claim 26, wherein said second DMA transfer is initiated after said data transfer to said buffer memory is terminated.

34.   The apparatus of claim 26, wherein said device and said main memory are decoupled.

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